Ultra-Low Voltage Datapath Blocks in 28nm UTBB FD-SOI

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***Abstract*—This paper demonstrates a wide supply range multiply-accumulate datapath block in 28nm UTBB FD-SOI technology. Variability and leakage reduction strategies are employed in this new technology to achieve a state-of-the-art low energy performance. The design uses a wide range of supply voltages to reduce energy consumption per operation. The extensive back-gate biasing range allows to adapt the minimum energy point (MEP) of the circuit to the desired workload. Measurements showcase the speed/energy trade-off of both the design and the technology and lead to a MEP of $0.17\mathrm{pJ}$ at $35\mathrm{MHz}$ with a supply voltage of $250\mathrm{mV}$ and a back-gate bias of $0.5\mathrm{V}$.**

I. Introduction

The processing capability of battery powered devices in mobile and biomedical applications is severely limited by the required battery autonomy. Especially DSP datapath blocks with a high activity are considered in this regard. As the active energy of digital circuits decreases with ${V_{\mathrm{dd}}}^2$, reducing the supply voltage is a very effective way of saving energy. As shown in [1], minimum energy operation is achieved at supply voltages near the threshold voltage. Scaling down the supply voltage is limited by variability and drive current of devices at these supplies. [2] shows very good circuit techniques to cope with these variations while maintaining reasonable clock speed and displays high energy savings in datapath blocks. The development of more advanced CMOS technologies leads to increased performance in speed. However, the increasingly smaller dimensions of these technologies also pose more severe restrictions on robustness against variability and process variations. Furthermore, most technologies leave V_{dd} as the only tweaking parameter for operation in multiple operating modes. This is sub-optimal for energy consumption, since operation outside the MEP is necessary. Meanwhile, the demand for multiple operating modes increases exponentially due to the integration of smart sensor nodes in various applications.

In this work, we explore the potential of Ultra Thin Buried-Box Fully Depleted Silicon-On-Insulator (UTBB FD-SOI) technology to cope with these restrictions in an advanced 28nm technology node. The fully depleted channel of devices in this technology improves variability, while the ultra-thin buried oxide diminishes leakage current and allows back-gate biasing. With a V_{t}-modulation of $85\mathrm{mV/V}$ [3] using the back-gate, switching between low power slow or high power fast performance is easily possible. A multiply-accumulate block (MAC) [4] is ported to this technology in order to assess the low voltage design concept for 28nm UTBB FD-SOI. Extensive speed and energy measurements of multiple dies over a large range of supply voltages and back-gate biasing voltages are reported. The applied strategy results in a state-of-the-art low energy consumption.

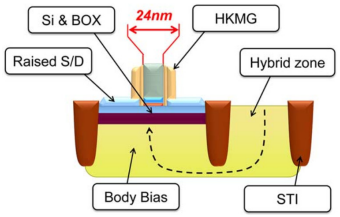

Fig. 1. UTBB FD-SOI transistor cross-section [3].

Section II takes a closer look to the properties of UTBB FD-SOI technology and its benefits. Section III assesses the technology for near-threshold operation, while section IV discusses the design considerations made for the MAC in 28nm and how it was realized with a convenient design flow. Finally, section V discusses the extensive measurements which were performed.

II. UTBB FD-SOI Technology Overview

28nm UTBB FD-SOI is a technology that has recently come available for designers around the world. It has promising properties for ultra-low power digital systems due to its decreased leakage and variability, and its wide back-gate biasing range. A cross-section of an UTBB FD-SOI transistor is shown in Fig. 1. It employs an ultra-thin (25nm) buried oxide (BOX) to dielectrically isolate the transistor from the back-gate. This results in reduced drain/source-substrate parasitic capacitances, lower leakage and latch-up immunity [3]. Using the back-gate, a V_{t} modulation of 85mV/V is achieved, which is limited only by the forward junction ($-0.3\mathrm{V}$, reverse back-gate biasing) and the breakdown ($+3\mathrm{V}$, forward back-gate biasing) voltage. It allows to adapt the leakage and speed of the circuit to the application. The FD technology does not require doping implants in the channel, which means the channel does not suffer from random dopant fluctuation (RDF) effects. Therefore variability is significantly reduced. The diminished short channel effects (SCE) allow the channel to be shrunk to 24nm. Due to the FD channel, multi-V_{t} devices are not realized by multiple dopant levels. The difference between Regular V_{t} (RVT) and Low V_{t} (LVT) devices is enabled by differently

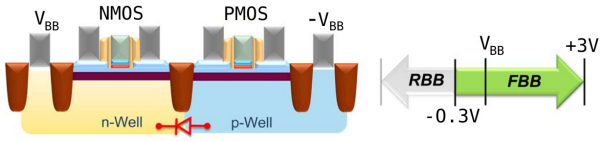

Fig. 2. UTBB FD-SOI transistor LVT flip-well configuration with back-gate biasing range [3].

doping the wells underneath the BOX. As is shown in Fig. 2 the LVT devices employ a flip-well configuration, which is possible because of the isolating oxide between the channel and the well. As discussed in [3], this modulates the FD channel to meet the LVT standard. Of course this introduces issues when mixing different V_{t}-flavours. To compensate for this void, the technology offers a way of modulating the gate length, called poly-biasing (PB). PB allows to adapt the channel length of a single transistor from 24nm up to 40nm at design time. There is no influence on the drawn gate length, which is convenient to intervene in existing cells. In this way the designer can use a limited amount of cells and vary its leakage properties with a factor 10 or more throughout the design without redrawing the complete cell. This results in a significant speedup at design time. All these characteristics make it interesting to use this technology for ultra-low power digital circuits.

III. Ultra-Low Voltage Operation

To assess the improvement 28nm UTBB FD-SOI brings for ultra-low voltage operation, several key transistor characteristics were simulated. In this section energy, speed and variability are investigated for operation down to the lowest supply voltage possible. The simulations confirm the characteristics as discussed in section II and are fundamental for the implemented circuit in section IV.

A. Energy

The goal of ultra-low voltage operation is to reduce active energy, since it decreases with ${V_{\mathrm{dd}}}^2$. To facilitate this, transistors need to be able to be switched on at low V_{gs}. The choice for the LVT-flavour is therefore straightforward. Circuit techniques to decrease the higher leakage of these devices are necessary. An important benefit of the LVT configuration is extreme forward back-gate biasing: it enables the designer to reduce the V_{t} even further, decreasing the lowest supply voltage to the bare minimum. It can be used to adjust the MEP to the workload, creating ideal conditions for a variety of operating modes. Decreasing the V_{t} using the back-gate again increases leakage, but is possible due to the good leakage properties of this SOI technology. A fully symmetrical back-gate biasing scheme is applied. The V_{bs} of the NMOS is applied with V_{BB}. The V_{bs} of the PMOS is adjusted accordingly to -V_{BB}. First of all, this results in a difference in V_{bs} between NMOS and PMOS devices. Secondly, when decreasing the supply voltage, the PMOS V_{bs} decreases. Since V_{bs} is the modulating voltage, this weakens the PMOS devices, resulting in a decreased $\mathrm{I_{drive,n}}/\mathrm{I_{drive,p}}$-ratio which slightly

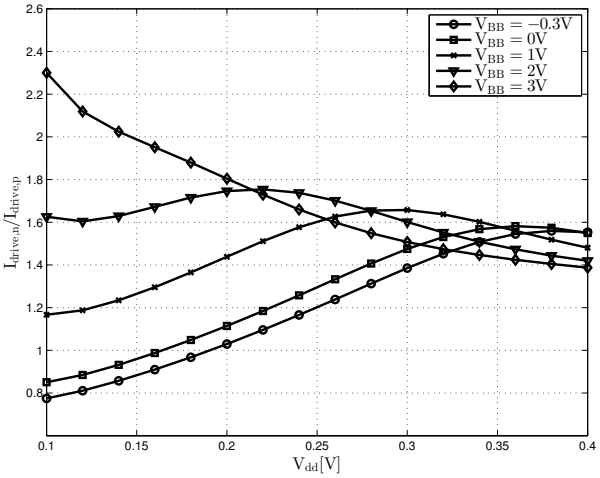

Fig. 3. $\mathrm{I_{drive,n}}/\mathrm{I_{drive,p}}$ ratio as a function of V_{dd} for varying V_{BB}.

decreases the performance. [5] shows this effect is limited in the proposed voltage supply range. Asymmetrical back-gate biasing can reduce this effect if necessary.

B. Speed

To operate circuits at ultra-low supply voltages means transistors will be operating in or near the weak inversion region. An important consideration of such operation is the relation between the NMOS and PMOS drive current ($\mathrm{I_{drive,n}}$ and $\mathrm{I_{drive,p}}$). In bulk CMOS, PMOS strength typically decreases with decreasing supply voltage, which is detrimental for the $\mathrm{I_{drive,n}}/\mathrm{I_{drive,p}}$-ratio. As a consequence, equal delay sizing for low voltage supplies typically leads to big PMOS transistors, as described in [2]. Fig. 3 shows $\mathrm{I_{drive,n}}/\mathrm{I_{drive,p}}$ for voltages up to $400\mathrm{mV}$ for an inverter with a PMOS/NMOS-ratio of 2. Equal drive current is achieved at supply voltages around $200\mathrm{mV}$. High V_{BB} increases the $\mathrm{I_{drive,n}}/\mathrm{I_{drive,p}}$-ratio at the lowest supply voltages due to the difference in V_{bs} between both devices. An asymmetrical back-gate bias could individually modulate NMOS and PMOS strength, but is not considered here since it would constrain back-gate biasing during circuit operation. In principle, minimum operating voltage is only limited by these currents. However, the exponential subthreshold slope of the current in this operating region is highly susceptible to variation and therefore imposes a limit on the lowest operating voltage.

C. Variability

Under process variations, the minimal supply voltage is limited by the minimal $\mathrm{I_{drive,n}}$ and $\mathrm{I_{drive,p}}$ still high enough to facilitate correct operation. When confronted with variations, overall $\mathrm{I_{drive,n}}$ and $\mathrm{I_{drive,p}}$ degrade severely. Fig. 4 shows the σ/μ-ratio for both drive currents of an inverter with PMOS/NMOS-ratio of 2. Although UTBB FD-SOI has characteristics that decrease variability (see section II), intra-die variations at low supply voltage are still substantial. Starting from $300\mathrm{mV}$, both σ/μ-ratios improve significantly. Operation below this voltage therefore requires circuit techniques to

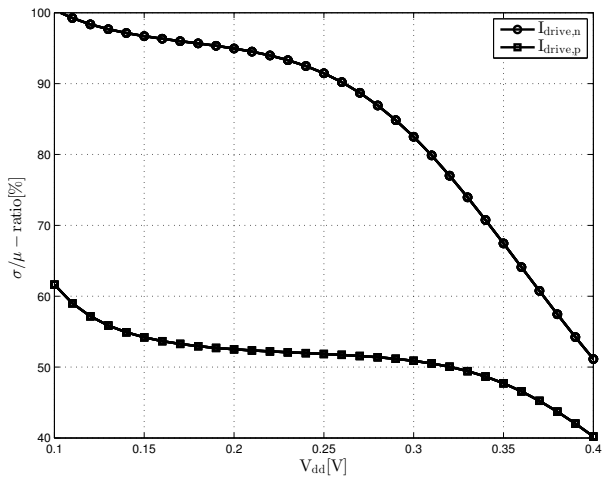

Fig. 4. Intra-die variation of $I_{drive,n}$ and $I_{drive,p}$ (1000MC).

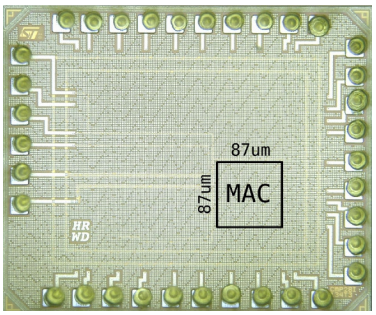

Fig. 5. Chip micrograph of the 28nm UTBB FD-SOI MAC.

TABLE I
ANALYSIS OF MINIMUM ENERGY OPERATION.

Technology	[4] 90nm bulk	This work 28nm UTBB FD-SOI				
Operation Mode	MEP	$V_{dd,min}$	MEP	MEP @ no V_{BB}	MEP @ $V_{BB,min}$	MEP @ $V_{BB,max}$
V_{dd}[V]	0.19	**0.21**	0.25	0.29	0.33	0.29
V_{BB}[V]	/	1.0	0.5	**0.0**	−0.3	1.5
Speed[MHz]	10	8.5	35	25	26	**147**
$P_{leak}[\mu W]$	3.90	5.67	2.13	0.95	**0.65**	33.52
E_{tot}[pJ]	0.87	1.04	**0.17**	0.28	0.32	0.42

reduce variation. The techniques discussed in [2] are highly effective to accomplish this and are implemented in the design discussed in section IV.

IV. Circuit-Level Benchmarking

A. Multiply-Accumulate

A 16bit Modified Baugh-Wooley Multiply-Accumulate unit was implemented in accordance to the design strategy explained in [4]. It uses transmission gate logic and employs a latch-based deep pipeline for high throughput data rate. The transmission gates decrease the leakage and the susceptibility to process variations, while the latch-based pipeline allows time borrowing to compensate for varying path delays. Functional verification of the circuit was done at SPICE level, while circuit layout was completed with commercial place-and-route tools using custom designed standard cells. This enables a significant speed-up in design time compared to [4], while still outperforming the full custom work. The extensive metal stack allows separate back-gate contacts with no area overhead, to easily facilitate back-gate biasing.

B. Minimal Supply & Energy Optimization

Section III showed the restrictions caused by $I_{drive,n}/I_{drive,p}$ and intra-die variability. For operation at lowest supply voltages equal drive currents are required. A PMOS/NMOS width ratio of 2 is chosen to accomodate this. The relatively small PMOS size allows a small circuit layout and is a benefit of this technology compared to bulk CMOS. A PB of $4nm$ is employed to decrease leakage, resulting in a physical gate length of $28nm$. Since back-gate biasing is adjustable during measurements, no definitive back-gate bias scheme was chosen at design time. This configuration results in state-of-the-art energy results, as shown in section V.

V. Measurements

Fig. 5 shows the chip micrograph. Active area is only $84x84\mu m^2$. A total of 3 dies was measured. Fig. 6 shows the mean performance in speed of the measured dies for a supply range up to 400mV and back-gate bias (V_{BB}) from $-0.3V$ up to $1.5V$. Note that in reverse back-gate biasing, the well junction is almost forward biased ($0.6V$). The power consumed by the back-gate in this operating mode was measured to be $12.3\mu W$. This power was not taken into account for energy calculations. Table I shows that the design is fully functional down to a supply voltage of $210mV$ with an energy consumption of $1.04pJ$/operation at a speed of $8.5MHz$ and a back-gate bias of $1V$. Back-gate biasing up to $V_{BB} = 1V$ significantly increases operating speed for the same supply voltage. Higher back-gate biasing reduces the V_t to the amount that speed increase is diminished.

Energy consumption at maximum speed for each supply voltage and back-gate bias is shown in Fig. 7. Both extreme reverse and extreme forward back-gate bias increase the energy per operation (table I), while moderate back-gate bias ($V_{BB} = 0..1V$) reduces energy per operation to its minimum. The MEP of $0.17pJ$ is achieved at $250mV$ with $V_{BB} = 0.5V$ at a frequency of $35MHz$. Varying back-gate bias allows different MEPs according to the performance requirements of the circuit. When no back-gate bias is applied, supply voltage at the MEP is increased, speed is degraded and energy consumption is increased. Although this work's $V_{dd,min}$ is higher, it outperforms [4] both in speed and energy, even when no back-gate bias is applied. The energy reduction that is achieved with back-gate biasing should be compared with the drawback of generating the voltages which need to be applied due to back-gate biasing.

Fig. 8 shows a contour plot of the energy per operation at $35MHz$ for a variety of supply and back-gate bias voltages. Energy was measured for supplies up to $400mV$ and for back-gate bias up to $1.5V$. In table II, a few configurations on how to achieve $35MHz$ operation are displayed. Both lower supplies

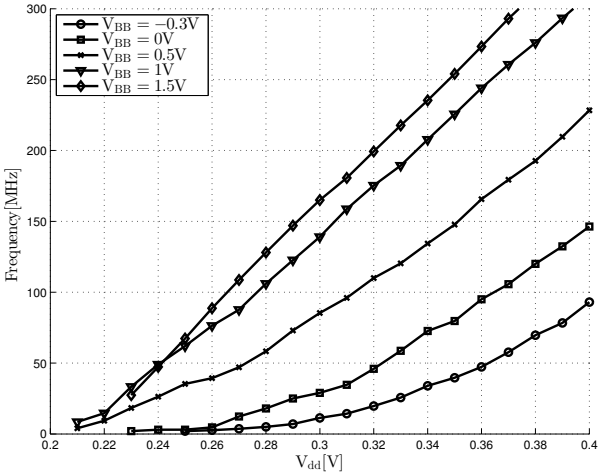

Fig. 6. Measured clock frequency as a function of the supply voltage for multiple back-gate biasing voltages.

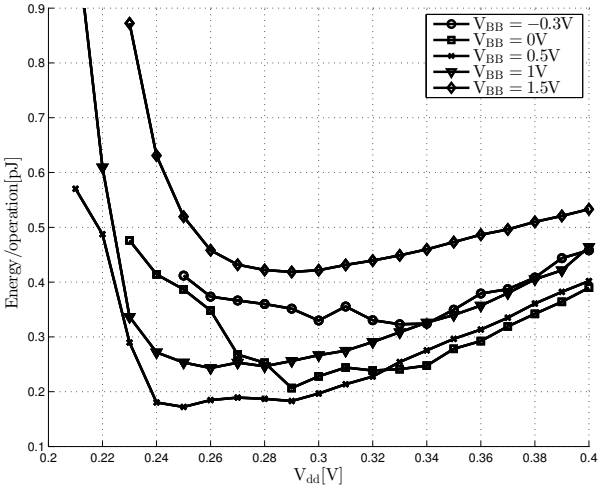

Fig. 7. Measured energy as a function of the supply voltage for multiple back-gate bias voltages.

TABLE II
ANALYSIS OF 35MHz OPERATION.

Specs @ 35MHz	$V_{\mathrm{dd,min}}$	MEP	no V_{BB}	$V_{\mathrm{BB,min}}$	$V_{\mathrm{BB,max}}$
V_{dd}[V]	0.23	0.25	0.31	0.34	0.24
V_{BB}[V]	1.0	0.5	0.0	−0.3	1.5
$\mathrm{P_{leak}}[\mu\mathrm{W}]$	9.53	2.13	1.09	0.70	27.14
$\mathrm{E_{tot}}$[pJ]	0.36	0.17	0.24	0.33	0.78

and higher back-gate bias significantly increase the leakage power, which is detrimental for the total energy. The MEP marks the optimal V_{BB} - V_{dd} configuration for this speed. When no back-gate bias is applied, 35MHz can be achieved at a supply voltage of $310\mathrm{mV}$ at the cost of $0.24\mathrm{pJ}$ per operation. At this speed, back-gate biasing therefore reduces energy with almost 30%.

VI. CONCLUSION

This paper presents a circuit concept for ultra-low voltage datapath blocks in 28nm UTBB FD-SOI. LVT devices are used to decrease the voltage supply, while transmission gates and latch-based deep pipelining handle process variations at these low supplies and reduce leakage even further. The design concept is successfully implemented in a 16bit MAC that reaches a state-of-the-art low energy consumption of $0.17\mathrm{pJ}$ at $250\mathrm{mV}$ with $V_{\mathrm{BB}} = 0.5\mathrm{V}$ at a speed of $35\mathrm{MHz}$. The extensive measurement results show the trade-off between back-gate bias and voltage scaling: forward back-gate bias up to $V_{\mathrm{BB}} = 0.5\mathrm{V}$ decreases the total energy, especially at low voltage supplies. Any higher forward back-gate bias increases energy consumption due to high leakage. Reverse back-gate biasing is highly effective to reduce leakage at the cost of speed.

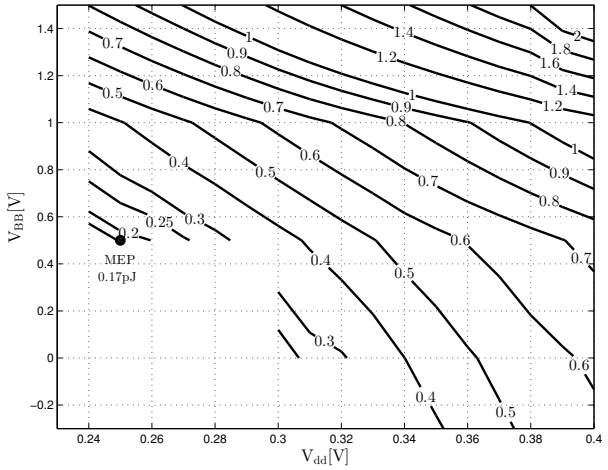

Fig. 8. Contour plot of the measured energy/operation [pJ] at 35MHz as a function of V_{dd} and V_{BB}.

ACKNOWLEDGMENT

This work was funded by the IWT - agency for Innovation by Science and Technology, and ST Microelectronics. The author would like to thank Andreia Cathelin, Didier Belot and Phillipe Flatresse from ST Microelectronics for their valuable contributions and support.

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